IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Attorney Docket No. 13912US04)

In the Application of:

Ichiro Fujimori

Serial No. 10/801,260

Filed: March 15, 2004

For: SYSTEM AND METHOD TO REDUCE NOISE IN A SUBSTRATE

Examiner: Phat X. Cao

Group Art Unit: 2814

Confirmation No. 2251

Electronically Filed on 14-JAN-2008

REPLY BRIEF

MS: APPEAL BRIEF-PATENTS
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 CFR 41.41, the Appellant submits this Reply Brief in response to the Examiner's Answer mailed on November 15, 2007. Claims 1-15 are pending in the present Application. The Appellant has responded to the Examiner in the Examiner's Answer, as found in the following Argument section.

As may be verified in his final Office Action (pages 2-5), dated November 28, 2006 ("Final Office Action"), claims 1, 8-9, 12 and 14-15 stand rejected under

35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,356,497, issued to Puar et al. (hereinafter, Puar), in view of U.S. Patent No. 6,395,591, issued to McCormack et al. (hereinafter, McCormack). Claims 1-10, 12 and 14-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McCormack in view of Puar. Claims 11 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McCormack and Puar as applied to claim 1, and further in view of U.S. Patent No. 6,403,992, issued to Wei (hereinafter, Wei). Claims 1-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wei in view of Puar. To aid the Board in identifying corresponding arguments, the Appellant has used the same headings in the Argument section of this Reply Brief as the headings found in the Appellant's corresponding Brief on Appeal. The Brief on Appeal has a date of deposit of August 15, 2007.

STATUS OF THE CLAIMS

Claims 1-15 were finally rejected. Pending claims 1-15 are the subject of this appeal.

ARGUMENT

I. The Proposed Combination of Puar and McCormack Does Not Render Claims 1, 8-9, 12 and 14-15 Unpatentable (Pages 2-3 of the Final Office Action

The Examiner has withdrawn the rejections over Puar in view of McCormack in order to simplify the issues to the appeal. Therefore, the Appellant's arguments on pages 6-11 of the Appeal Brief with regards to the rejections as being unpatentable over Puar in view of McCormack are moot.

II. The Proposed Combination of McCormack and Puar Does Not Render Claims 1-10, 12 and 14-15 Unpatentable (Pages 3-4 of the Final Office Action)

II.A. Rejection of Claim 1

The Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

In response to Appellant's Brief on Appeal, the Examiner initially states the following on pages 7-11 of the Examiner's Answer:

> With regarding to the rejection of independent claim 1 as being unpatentable over McCormack in view of Puar (Section 3 of Final Office Action), Appellant (pages 12-14 of Brief) first asserts that the Final Office Action states at pages 2-3 that:
>
> "However, McCormack (Fig. 2) teaches the forming of a transistor within a transistor well layer and on a lightly doped (p-) substrate layer 50. The transistor well layer is isolated or shielded from the substrate 50 by a p type epitaxy layer 12 disposed therebetween. **The layer 12 functions as a shielding layer for reducing the noise in the chip because it isolates the substrate 10 from the**

> **transistor layer and has a higher doping than the underlying substrate 10 for providing immunity against parasitic substrate effects or latchup effects (column 1, lines 19-24 and column 4, lines 9-13)**. Accordingly, it would have been obvious to modify the device of Puar by forming the shielding layer between the substrate layer and the transistor well layer because such forming of the low resistivity shielding layer would isolate the noise transfer to the transistor layer by reducing parasitic substrate effects or latchup effects. (emphasis added)". (see page 13 of Brief).
>
> Appellant then concludes that the combination of McCormack and Puar does not suggest the invention as claimed because "the above bolded statement by the Examiner... is completely erroneous and is not supported by McCormack" (page 13 of Brief).
>
> Appellant is advised to review the Final Office Action again because the Examiner believes that Appellant is erroneous. Appellant is erroneous because the above cited paragraph of the Final Office Action is in the ground of rejection of Puar in view of McCormack, but not in the ground of rejection of McCormack in view of Puar (Section 3, pages 3-4 of Final Office Action). The Examiner thus submits that Appellant has failed to address the rejection of claim 1 under the ground of rejection of McCormack in view of Puar.

The Appellant realizes that the above cited paragraph of the Final Office Action is in the ground of rejection of Puar in view of McCormack, but not in the ground of rejection of McCormack in view of Puar. However, since **the above cited paragraph is the only place in the Final Office Action where the Examiner has discussed his reasoning as to why "layer 12 functions as a shielding payer for reducing the noise in the chip,"** the Appellant has used

the relevant portion of Examiner's own argument for purposes of demonstrating why layer 12 cannot function as a shielding layer for reducing noise in the chip.

Therefore, the Appellant maintains the arguments stated in pages 12-14 of the Brief that layer 12 of McCormack does not act as a shielding layer for reducing noise in the chip.

The Examiner further states the following in pages 8-9 of the Examiner's Answer:

> With further regarding to the rejection of claim 1, Appellant (pages 15-16 of Brief) argues that in Fig. 2 of McCormack, the layer 12 disposed between the substrate 10 and the transistor well layer 16/18/22 would not function as "a shielding layer" for reducing "transfer of noise in the chip".
>
> This argument is not persuasive because of the following reasons:
>
> First, one skill in the art would have no difficulty to recognize that **the P-type layer 12 would function as "a shielding layer" for reducing the noise transfer from the transistor well regions to the substrate 10 because the layer 12 disposed between the substrate 10 and the transistor well regions to isolate the substrate from the well regions**.

The Appellant respectfully disagrees with the above bolded statement by the Examiner. **As clearly illustrated in FIG. 2 of McCormack, the layer 12 continuity is disrupted by the p++ region 14 (which borders P-well 16 and substrate 10), so that the well regions 16-22 are not isolated by the layer 12 from the substrate 10. Instead, region 14 isolates at least the P-well 16 from layer 10.**

Examiner further states the following in pages 10-11 of the Examiner's Answer:

> Clearly, Fig. 2 of McCormack also has the capacitive coupling formed by P and N junctions of the P-doped layer 12 and the N-Well layer 22 and the resistive coupling formed by P and P junctions of the P-doped layer 12 and the P-Well layer 18. Therefore, **the P-doped layer 12 shown in Fig. 2 of McCormack would also function as a shielding layer for reducing the noise** in the N-Well 22 and the noise in the P-Well 18 to reach the P- doped substrate 10 **because of the junction capacitive coupling formed between the P-doped layer 12 and the N-Well layer 22 and the resistive coupling formed between the P-doped layer 12 and the P-Well layer 18.**

The Appellant respectfully disagrees with the above bolded statement by the Examiner. Initially, the Appellant points out that **the Examiner has not addressed the Appellant's arguments stated in pages 15-16 of the Brief on Appeal.** For example, the Examiner has relied, in the Final Office Action and the Advisory Office Action, on latchup susceptibility and layer doping to support his assertion that the shielding layer 12 of McCormack also reduces noise in the chip. The Appellant, therefore, maintains the arguments stated in pages 15-16 of the Brief on Appeal.

Based on the above bolded argument from pages 10-11 of the Examiner's Answer, **it seems that the Examiner is now using a new argument for support of his assertion that the shielding layer 12 of McCormack also reduces noise in the chip. Initially, the Appellant points out that McCormack does not disclose any of the resistive or capacitive couplings**

stated in the Examiner's argument above. Even if we assume for the sake of argument that McCormack discloses resistive and capacitive couplings, the Examiner's argument is still deficient. For example, there is absolutely no support in McCormack layer 12, shown in Fig. 2 of McCormack, would also function as a shielding layer for reducing the noise simply because of the alleged resistive and capacitive couplings. In addition, the Examiner has not provided any explanation of why the alleged resistive and capacitive couplings of McCormack will, in fact, cause the layer 12 to reduce the noise in the chip.

The Appellant respectfully submits that independent claim 1 is allowable.

II-C. Rejections of Dependent claims 2-3

The Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

The Appellant respectfully submits that dependent claims 2-3 are allowable.

II-D. Rejection of Dependent Claim 4

The Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

In response to Appellant's Brief on Appeal, the Examiner initially states the following on pages 11-12 of the Examiner's Answer:

> From the statement above, "at least one transistor of said second transistor type" as claimed refers to "a transistor 28 of a second transistor type (N type)" shown in Fig. 2 of McCormack, and "said transistor layer" as claimed refers to "the transistor well layer 16". Clearly, the transistor 28 of a second transistor type (N type) is disposed within the transistor well layer 16. Therefore, Appellant's argument is not persuasive because Fig. 2 of McCormack clearly discloses "at least one transistor of said second transistor type is disposed within said transistor layer," as recited by the Appellant in claim 4.

The Appellant disagrees and points out that claim 4 depends on claim 2. Furthermore, **even though transistor 28 may be disposed within well 16, the transistor 28 is <u>not</u> coupled to the shielding layer 12, as clearly seen from FIG. 2 of McCormack.**

The Appellant respectfully submits that dependent claim 4 is allowable.

<u>II-E. Rejection of Dependent Claim 5</u>

The Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

In response to Appellant's Brief on Appeal, the Examiner initially states the following on pages 12-14 of the Examiner's Answer:

> With regard to the rejection of dependent claim 5, Appellant (pages 18-19 of Brief, Section E) argues that Fig. 2 of McCormack does not disclose "said at least one transistor of said second transistor type is resistively coupled to said shielding layer," as claimed.
>
> It is noted that the limitation "said at least one transistor of said second transistor type is resistively coupled to said shielding

layer" refers to resistive coupling 180 shown in **Fig. 2 of Appellant below** (also see Applicant's specification, par. [11]), the resistive coupling 180 is formed by P-P junctions of the P-well 110 and the P+ diffusion B and it is resistively coupled to the shielding layer 80 through the P-well 110.

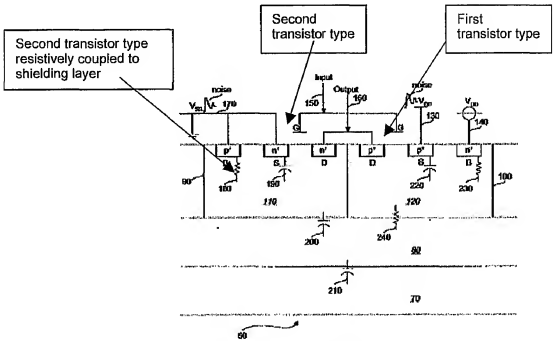


FIG. 2.

The Appellant respectfully disagrees with the Examiner's interpretation above of Appellant's FIG. 2. **For example, the Examiner is referred to ¶ 20 of the present application, where it is explained that the resistive coupling 180 is used to couple the body terminal of transistor 90 to the p-well 110, and the resistive coupling 180 is not used to couple a transistor to the shielding layer 90. As clearly seen from Appellant's FIG. 2, it is the resistive coupling 240 (which couples transistor 100 to the shielding layer 80), and not**

resistive coupling 180, which satisfies the limitations of Appellant's claim 5.

The Examiner further states the following in pages 13-14 of the Examiner's Answer:

Now, referring to **Fig. 2 of McCormack** below,

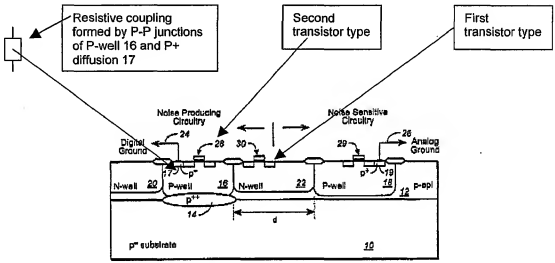


FIG._2

Fig. 2 of McCormack above clearly teaches a resistive coupling which is formed by P-P junctions of the P-well 16 and the P+ diffusion 17 and it is resistively coupled to the shielding layer 12 through the P-well 16. Therefore, Appellant's argument in regard to the rejection of claim 5 is not persuasive because Fig. 2 of McCormack clearly discloses "said at least one transistor [28]of said second transistor type [N type] is resistively coupled to said shielding layer [12]" through the P-well 16.

The Appellant disagrees. Initially, the Appellant points out that McCormack does not disclose any resistive coupling between the P-well 16 and

the P+ diffusion 17. Even if we assume for the sake of argument that there is resistive coupling between the P-well 16 and the P+ diffusion 17 of McCormack, the Examiner's argument is still deficient. The Appellant points out that, **as clearly seen from the above FIG. 2 of McCormack, any resistive coupling between the P-well 16 and the P+ diffusion 17 will not go beyond the well 16 and will not couple the transistor 16 to the shielding layer 12.**

The Appellant respectfully submits that dependent claim 5 is allowable.

II-F. Rejection of Dependent Claims 6-7

The Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

In response to Appellant's Brief on Appeal, the Examiner initially states the following on pages 14-15 of the Examiner's Answer:

> With regard to the rejection of claims 6-7, the Final Office Action states:
>
> "Regarding claims 6-7, McCormack (Fig. 2) further discloses a transistor 28 of a second transistor type (N type) ... has a first noisy voltage source 24 (column 3, lines 53-55) coupled to a source 17 of the transistor 28." (page 4 of Final Office Action)
>
> However, Appellant (pages 19-20 of Brief, Section F) argues that the terminal 24 coupled to the source 17 of the transistor 28 "is digital ground - it is not a noisy voltage source".
>
> This argument is not persuasive because McCormack clearly states at column 3, lines 53-55 and lines 62-64:
>
> "Also, the analog ground is sometimes referred to as the 'quiet ground' and the digital ground is sometimes referred to as the

> 'noisy ground' ... , the digital ground (terminal 24) including ground noise generated by the n-channel transistors of P-well 16 ... " [emphasis added].
>
> Therefore, the terminal 24 coupled to the source 17 of the transistor 28 is a "noisy" digital ground. Furthermore, **as defined by Appellant, a ground is a voltage source**. Specifically, Appellant states at paragraph [05], 'lines 7-8 of specification:
>
> "A voltage source Vss 7 having a ground ... ";
>
> and at paragraph [15], line 8:
>
> "A voltage source Vss 170 having an electrical ground... "

The Appellant disagrees. The Examiner has mischaracterized the present specification. **For example, ¶ 05 of the present specification states that the voltage source Vss 7 has a ground, as clearly seen in FIG. 1 of the present application. This is different from the Examiner's interpretation of "a ground is a voltage source," which is clearly erroneous as stated in the above argument. Furthermore, the above citation from McCormack (col. 3, lines 53-55, 62-64) relates to the ground terminal, and not to a voltage source or even to a noisy voltage source.**

The Appellant respectfully submits that dependent claims 6-7 are allowable.

II-H. Rejection of Dependent Claim 10

The Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

In response to Appellant's Brief on Appeal, the Examiner initially states the following on pages 16-17 of the Examiner's Answer:

> With regard to the rejection of dependent claim 10, Appellant (pages 20-21 of Brief, Section H) argues that Fig. 2 of McCormack does not disclose "said at least one transistor of said first transistor type is capacitive coupled to said shielding layer," as claimed.
>
> It is noted that the limitation "said at least one transistor of said first transistor type is capacitive coupled to said shielding layer" refers to capacitive coupling 220 shown in **Fig. 2 of Appellant below** (also see Applicant's specification, par. [11]), the capacitive coupling 220 is formed by P-N junctions of the N-well 120 and the P+ diffusion S and it is capacitive coupled to the shielding layer 80 through the N-well 120.

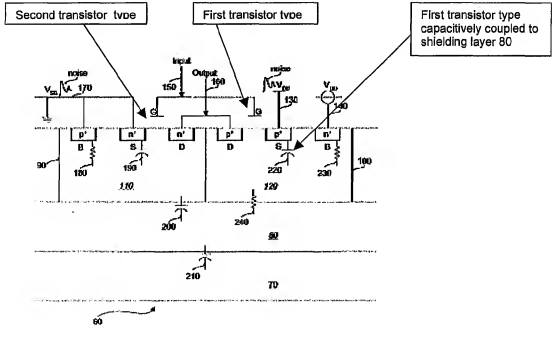


FIG. 2.

The Appellant respectfully disagrees with the Examiner's interpretation above of Appellant's FIG. 2. **For example, the Examiner is referred to ¶ 21 of the present application, where it is explained that the capacitive coupling**

220 is used to couple the source terminal of transistor 100 to the n-well 120, and the capacitive coupling 220 is not used to couple a transistor to the shielding layer 90. As clearly seen from Appellant's FIG. 2, it is the resistive coupling 200 (which couples transistor 90 to the shielding layer 80), and not capacitive coupling 220, which satisfies the limitations of Appellant's claim 10.

The Examiner further states the following in pages 16-17 of the Examiner's Answer:

Now, referring to **Fig. 2 of McCormack** below,

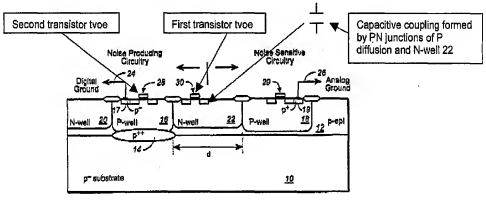


FIG._2

Fig. 2 of McCormack above clearly teaches a capacitive coupling which is formed by PN junctions of the P diffusion and the N-well 22 and it is capacitively coupled to the shielding layer 12 through the N-well 22. Therefore, Appellant's argument in regard to the rejection of claim 10 is not persuasive because Fig. 2 of McCormack clearly discloses "said at least one transistor [30]of said first transistor type [P type] is capacitively coupled to said shielding layer [12]" through the N-well 22.

The Appellant disagrees. Initially, the Appellant points out that McCormack does not disclose any capacitive coupling between the N-well 22 and the P diffusion of transistor 30. Even if we assume for the sake of argument that there is capacitive coupling between the N-well 22 and the P diffusion of transistor 30, the Examiner's argument is still deficient. The Appellant points out that, **as clearly seen from the above FIG. 2 of McCormack, any capacitive coupling between the N-well 22 and the P diffusion of transistor 30 will not go beyond the well 22 and will not couple capacitively the transistor 30 to the shielding layer 12.**

The Appellant respectfully submits that dependent claim 10 is allowable.

II-I. Rejection of Dependent Claim 12

The Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

The Appellant respectfully submits that dependent claim 12 is allowable.

II-H. Rejection of Dependent Claims 14 and 15

The Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

In response to Appellant's Brief on Appeal, the Examiner initially states the following on pages 17-19 of the Examiner's Answer:

Appellant (page 22 of Brief, Section J) argues that Puar does not

> suggest "a noisy voltage source coupled to said at least one transistor of a first transistor type" as claimed in claims 14 and 15 because the voltage source 38 shown in Fig. 5 is not "noisy voltage source".
>
> This argument is not persuasive because Appellant has not provide any reasons to support that the voltage source 38 shown in Fig. 5 is not a "noisy voltage source". It is noted that Puar clearly states at column 4, lines 59-63 that VDD shown in Fig. 5 is a "quiet-reference voltage". Therefore, the voltage source 38 is a "noisy voltage source" because it is not connected to "quiet-reference voltage" VDD.

The Appellant disagrees and points out that the fact that a voltage source is not connected to a quiet reference voltage does not necessarily mean that the voltage source is a noisy voltage source. **There is simply no support in any of the cited references that if a voltage source is not connected to a quiet reference voltage, then the voltage source is in fact a noisy voltage source.**

The Appellant respectfully submits that dependent claims 14-15 are allowable.

III. The Proposed Combination of McCormack, Puar and Wei Does Not Render Claims 11 and 13 Unpatentable

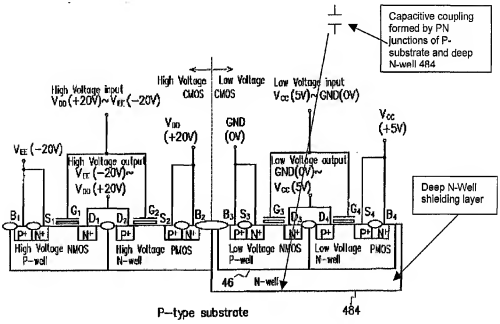
The Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

In response to Appellant's Brief on Appeal, the Examiner initially states the following on pages 18-19 of the Examiner's Answer:

> With regard to the rejections of claims 11 and 13, Appellant (page

23 of Brief) argues that it would not obvious to combine Wei with McCormack and Puar because Wei does not teaches that "said shielding layer is capacitively coupled to said substrate" (claim 11) and "said shielding layer is a deep N-well" (claim 13).

Appellant is advised to review the Wei reference again because **Fig. 4 of Wei** below clearly teaches the features above.



Therefore, Appellant's argument is not persuasive because Fig. 4 of Wei clearly suggests that the shielding layer 484 is a deep N-well and the shielding layer 484 of N type is formed a PN junction with and capacitively coupled to the substrate layer of P type. Thus, Fig. 4 of Wei does suggest the invention as claimed.

The Appellant disagrees. As seen from FIG. 4 of Wei, **484 is an N-well and it is not a shielding layer that shields the wells of the transistors from the substrate.** As seen from the above FIG. 4 of Wei, **the N-well 484 is in fact a partial N-well which does not even enclose all the wells (as seen from the above figure, the p-well and n-wells of the left two NMOS and PMOS**

transistors are not covered by the N-well 484). Needless to say, even if we assume that the N-well 484 is a "shielding layer", the Examiner's argument is still deficient as the N-well 484 does not support any of the limitations of the main independent claim 1 (e.g., as stated above, n-well 484 does not shield the entire transistor layer). Wei also does not disclose any capacitive coupling between the N-well 484 and the p-substrate.

The Examiner is also reminded that McCormack explicitly points out that a p-type epitaxy layer 12 is grown on the p-substrate 10. *See* McCormack, col. 2, line 66 – col. 3, line 4. Therefore, a capacitive coupling between a shielding layer and a substrate is not possible with the disclosed transistors of McCormack. A combination with Wei will change the principal of operation of McCormack. The Examiner is referred to the following MPEP citation:

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." M.P.E.P. § 2143.01(VI) at page 2100-130 (Rev. 5, Aug. 2006).

The Appellant respectfully submits that dependent claims 11 and 13 are allowable.

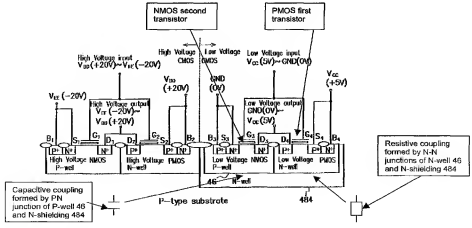
IV. The Proposed Combination of Wei and Puar Does Not Render Claims 1-13 Unpatentable

IV-A. Rejection of Claim 1

The Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

In response to Appellant's Brief on Appeal, the Examiner initially states the following on pages 20-21 of the Examiner's Answer:

> With regard to the rejection of independent claim1, Appellant (pages 24-25 of Brief) argues that Fig. 4 of Wei does not suggest "at least one transistor of a first transistor type that couples said transistor layer to said shielding layer" as claimed because item G4 is not a transistor, it is a ground terminal for the PMOS transistor.
>
> The Examiner recognizes that Appellant is erroneous because in **Fig. 4 of Wei below**, G4 terminal is not relied on for teaching as "at least one transistor of a first transistor type" as asserted by Appellant, but rather, the PMOS transistor (not labeled) connected to terminal G4 is relied on for teaching as "at least one transistor of a first transistor type".



The Appellant disagrees. Initially, as explained above, **the Appellant points out that the N-well 484 is not a shielding layer. Furthermore, referring to the above FIG. 4 of Wei, the PMOS transistor is within the N-well and it does not couple a transistor layer to the N-well 484, as seen from the above figure.**

The Appellant respectfully submits that independent claim 1 is allowable.

IV-B. Rejection of Dependent Claims 8 and 13

The Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

The Appellant respectfully submits that dependent claims 8 and 13 are allowable.

IV-C. Rejection of Dependent Claims 2-7

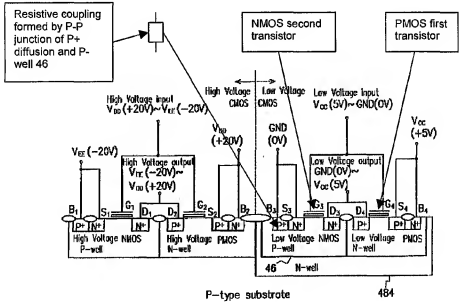
The Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

In response to Appellant's Brief on Appeal, the Examiner initially states the following on pages 21-24 of the Examiner's Answer:

> With regard to the rejections of dependent claims 2-7, Appellant (page 26 of Brief) argues that Fig. 4 of Wei does not suggest "one transistor of said second transistor type is disposed within said transistor layer" (claims 3-4) and "is resistively coupled to the shielding layer" (claims 2 and 5) because item G3 in Fig. 4 is a

ground terminal and not a transistor.

The Examiner recognizes that Appellant is erroneous because in **Fig. 4 of Wei below**, G3 terminal is not relied on for teaching as "one transistor of said second transistor type" as asserted by Appellant, but rather, the NMOS transistor (not labeled) connected to terminal G3 is relied on for teaching as "one transistor of said second transistor type".



It is noted that the limitation "said at least one transistor of said second transistor type is resistively coupled to said shielding layer" refers to resistive coupling 180 shown in **Fig. 2 of Appellant** (also see Applicant's specification, par. [11]), the resistive coupling 180 is formed by P-P junction of the P-well 110 and the P+ diffusion B and it is resistively coupled to the shielding layer 80 through the P-well 110.

The Appellant respectfully disagrees with the Examiner's interpretation above of Appellant's FIG. 2. **For example, the Examiner is referred to ¶ 20 of the present application, where it is explained that the resistive coupling 180**

is used to couple the body terminal of transistor 90 to the p-well 110, and the resistive coupling 180 is not used to couple a transistor to the shielding layer 90. As clearly seen from Appellant's FIG. 2, it is the resistive coupling 240 (which couples transistor 100 to the shielding layer 80), and not resistive coupling 180, which satisfies the limitations of Appellant's claim 5.

The Examiner further states the following in pages 22-23 of the Examiner's Answer:

> **Fig. 4 of Wei** above clearly teaches the NMOS second transistor type being disposed within the transistor layer 46, and a resistive coupling which is formed by P-P junction of the P+ diffusion and the P-well 46 and it is resistively coupled to the shielding layer 484 through the P-well 46. Therefore, Appellant's arguments in regard to the rejections of claims 2-5 are not persuasive because Fig. 4 of Wei clearly discloses" one transistor of said second transistor type [NMOS] is disposed within said transistor layer [46]" and "is resistively coupled to said shielding layer [484]" through the P-well 46.

The Appellant disagrees. Initially, the Appellant points out that Wei does not disclose any resistive coupling between the N-well 484 and the P-well 46. Even if we assume for the sake of argument that there is resistive coupling between the P-well 46 and the N-well 484, the Examiner's argument is still deficient. The Appellant points out that, **as clearly seen from the above FIG. 4 of Wei, any resistive coupling between the P-well 46 and the N-well 484 will not go beyond the P-well 46 and will not couple the NMOS transistor to the N-well 484.**

The Examiner further states the following in page 23 of the Examiner's Answer:

> Appellant (page 26 of Brief) further argues that the ground terminal GND of Wei coupled to the source S3 of the NMOS second transistor is not a noisy voltage source (claims 6-7).
>
> This argument is not persuasive because Appellant is reminded that as defined by Appellant, a ground is a voltage source. Specifically, Appellant states at paragraph [05], lines 7-8 of specification:
>
> "A **voltage source** Vss 7 having **a ground ...** ";
>
> and at paragraph [15], line 8:
>
> "A **voltage source** Vss 170 having **an electrical ground**... "
>
> It is noted that Appellant has not provide any reasons to support that the voltage source GND coupled to the source S3 of the NMOS is not a "noisy voltage source".

The Appellant disagrees. The Examiner has mischaracterized the present specification. **For example, ¶ 05 of the present specification states that the voltage source Vss 7 has a ground, as clearly seen in FIG. 1 of the present application. This is different from the Examiner's interpretation of "a ground is a voltage source," which is clearly erroneous as stated in the above argument. There is no support in any of the references that even if a voltage source is not connected to a quiet voltage source, then the voltage source is automatically a noisy voltage source.**

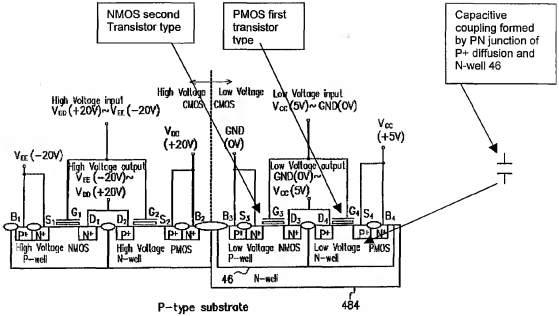
The Appellant respectfully submits that dependent claims 2-7 are allowable.

IV-D. Rejection of Dependent Claims 9-12

The Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

In response to Appellant's Brief on Appeal, the Examiner initially states the following on pages 24-26 of the Examiner's Answer:

> With regard to the rejections of dependent claims 9-12, Appellant (page 27 of Brief) argues that Fig. 4 of Wei does not suggest "one transistor of said first transistor type is disposed within said transistor layer" and "is capacitively coupled to the shielding layer" because item G4 in Fig. 4 is a ground terminal and not a transistor.
>
> The Examiner recognizes that Appellant is erroneous because in **Fig. 4 of Wei below**, G4 terminal is not relied on for teaching as "one transistor of said first transistor type" as asserted by Appellant, but rather, the PMOS transistor (not labeled) connected to terminal G4 is relied on for teaching as "one transistor of said first transistor type".



It is noted that the limitation "said at least one transistor of said first transistor type is capacitive coupled to said shielding layer" refers to capacitive coupling 220 shown in **Fig. 2 of Appellant** (also see Applicant's specification, par. [11]), the capacitive coupling 220 is formed by P-N junction of the N-well 120 and the P+ diffusion S and it is capacitive coupled to the shielding layer 80 through the N-well 120.

The Appellant respectfully disagrees with the Examiner's interpretation above of Appellant's FIG. 2. **For example, the Examiner is referred to ¶ 21 of the present application, where it is explained that the capacitive coupling 220 is used to couple the source terminal of transistor 100 to the n-well 120, and the capacitive coupling 220 is not used to couple a transistor to the shielding layer 90. As clearly seen from Appellant's FIG. 2, it is the resistive coupling 200 (which couples transistor 90 to the shielding layer**

80), and not capacitive coupling 220, which satisfies the limitations of Appellant's claim 10.

The Examiner further states the following in pages 25-26 of the Examiner's Answer:

> **Fig. 4 of Wei** above clearly teaches the PMOS first transistor type being disposed within the transistor layer 46, and a capacitive coupling which is formed by P-N junction of the P+ diffusion and the N-well 46 and it is capacitively coupled to the shielding layer 484 through the N-well 46. Therefore, Appellant's arguments in regard to the rejections of claims 9-12 are not persuasive because Fig. 4 of Wei clearly discloses" one transistor of said first transistor type [PMOS] is disposed within said transistor layer [46]" and "is capacitively coupled to said shielding layer [484]" through the N-well 46.

The Appellant disagrees. Initially, the Appellant points out that Wei does not specifically disclose any capacitive coupling between the P-N junction of the P+ diffusion and the N-well 46. Even if we assume for the sake of argument that there is capacitive coupling between the P-N junction of the P+ diffusion and the N-well 46, the Examiner's argument is still deficient. The Appellant points out that, **as clearly seen from the above FIG. 4 of Wei, any capacitive coupling between the P-N junction of the P+ diffusion and the N-well 46 will not go beyond the n-well 46 and will not couple capacitively the PMOS transistor of Wei to the N-well 484.**

The Appellant respectfully submits that dependent claims 9-12 are allowable.

CONCLUSION

The Appellant submits that the pending claims are allowable in all respects. Reversal of the Examiner's rejections for all the pending claims and issuance of a patent on the Application are therefore requested from the Board.

The Commissioner is hereby authorized to charge additional fee(s) or credit overpayment(s) to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Respectfully submitted,

Date: 14-JAN-2008

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